Customer No.: 31561
Application No.: 10/711,509
Docket No.: 12405-US-PA-0P

IN THE CLAIMS

Please amend the claims as follows.

1. (currently amended) A manufacturing method of a thin film transistor (TFT), comprising:

forming a gate over a substrate;

forming an inter-gate dielectric layer over the substrate covering the gate;

forming a channel layer over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer ~~comprises~~ is a lightly doped amorphous silicon layer; and

forming source/drain regions over the channel layer, wherein the source/drain regions are separated by a distance.

2. (original) The manufacturing method of claim 1, wherein the channel layer comprises an N-type lightly doped amorphous silicon layer.

3. (original) The manufacturing method of claim 1, wherein the channel layer comprises a P-type lightly doped amorphous silicon layer.

4. (original) The manufacturing method of claim 1, wherein the channel layer is doped with phosphorous atoms, and a concentration of phosphorous atoms is in a range of about 1E17 atom/cm^3 to about 1E18atom/cm^3.

5. (original) The manufacturing method of claim 1, wherein the channel layer is doped with boron atoms, and a concentration of boron atoms is in a range of about 1E16 atom/cm^3 to about 5E17 atom/cm^3.

6. (original) The manufacturing method of claim 1, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using

a reaction gas mixture comprising silane (SiH_4), hydrogen (H_2) and phosphine (PH_3), wherein a effective content ratio of the phosphine (PH_3) is in a range of about 2.8E-7 to about 8E-6, and wherein the effective content ratio of the phosphine (PH_3) is equal to the ratio of the content of phosphine (PH_3) to the total content of silane (SiH_4), hydrogen (H_2) and phosphine (PH_3).

7. (original) The manufacturing method of claim 1, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using a reaction gas mixture comprising silane (SiH_4), hydrogen (H_2) and boroethane (B_2H_6), wherein a effective content ratio of the boroethane (B_2H_6) is in a range of about 5E-7 to about 1E-5, and wherein the effective content ratio of the boroethane (B_2H_6) is equal to the ratio of the content of boroethane (B_2H_5) to the total content of silane (SiH_4), hydrogen (H_2) and boroethane (B_2H_6).

8. (original) The manufacturing method of claim 1, wherein the step of forming the channel layer comprises:

forming a first lightly doped sub-amorphous silicon layer over the portion of the inter-gate dielectric layer at a first deposition rate; and

forming a second lightly doped sub-amorphous silicon layer over the first lightly doped sub-amorphous silicon layer at a second deposition rate, wherein the first deposition rate is lower than the second deposition rate.

Claim 9 (cancelled)

10. (original) The manufacturing method of claim 1, further comprising a step of forming a protection layer over the substrate after the step of forming the source/drain regions covering the source/drain regions, the channel layer and the inter-

gate dielectric layer.

Claims 11-18 (cancelled)

19. (new) A manufacturing method of a thin film transistor (TFT), comprising:

forming a gate over a substrate;

forming an inter-gate dielectric layer over the substrate covering the gate;

forming a channel layer over a portion of the inter-gate dielectric layer at least over the gate, wherein the channel layer comprises a lightly doped amorphous silicon layer;

forming an ohmic contact layer over the channel layer; and

forming source/drain regions over the channel layer, wherein the source/drain regions are separated by a distance.

20. (new) The manufacturing method of claim 19, wherein the channel layer comprises an N-type lightly doped amorphous silicon layer.

21. (new) The manufacturing method of claim 19, wherein the channel layer comprises a P-type lightly doped amorphous silicon layer.

22. (new) The manufacturing method of claim 19, wherein the channel layer is doped with phosphorous atoms, and a concentration of phosphorous atoms is in a range of about 1E17 atom/cm^3 to about 1E18atom/cm^3.

23. (new) The manufacturing method of claim 19, wherein the channel layer is doped with boron atoms, and a concentration of boron atoms is in a range of about 1E16 atom/cm^3 to about 5E17 atom/cm^3.

24. (new) The manufacturing method of claim 19, further comprising a step of forming a protection layer over the substrate after the step of forming the source/drain

regions covering the source/drain regions, the channel layer and the inter-gate dielectric layer.

25. (new) The manufacturing method of claim 19, wherein the step of forming the channel layer comprises:

forming a first lightly doped sub-amorphous silicon layer over the portion of the inter-gate dielectric layer at a first deposition rate; and

forming a second lightly doped sub-amorphous silicon layer over the first lightly doped sub-amorphous silicon layer at a second deposition rate, wherein the first deposition rate is lower than the second deposition rate.

26. (new) The manufacturing method of claim 19, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using a reaction gas mixture comprising silane (SiH_4), hydrogen (H_2) and phosphine (PH_3), wherein a effective content ratio of the phosphine (PH_3) is in a range of about 2.8E-7 to about 8E-6, and wherein the effective content ratio of the phosphine (PH_3) is equal to the ratio of the content of phosphine (PH_3) to the total content of silane (SiH_4), hydrogen (H_2) and phosphine (PH_3).

27. (new) The manufacturing method of claim 19, wherein the step of forming the channel layer comprises performing a chemical vapor deposition (CVD) process using a reaction gas mixture comprising silane (SiH_4), hydrogen (H_2) and boroethane (B_2H_6), wherein a effective content ratio of the boroethane (B_2H_6) is in a range of about 5E-7 to about 1E-5, and wherein the effective content ratio of the boroethane (B_2H_6) is equal to the ratio of the content of boroethane (B_2H_6) to the total content of silane (SiH_4), hydrogen (H_2) and boroethane (B_2H_6).